WHAT IS CLAIMED IS:

1. A method of forming a metal on metal capacitor structure for an integrated circuit device, the method comprising:

forming a dual damascene structure, where the structure has a first conductive portion comprising copper material that is separated by a dielectric material from a second conductive portion, the second conductive portion is coupled to the first conductive portion underlying the dielectric material through a third conductive portion, the first conductive portion, the dielectric material, and the second conductive portion forming a substantially planar surface region opposing the third conductive portion, the first conductive portion and the second conductive portion coupled through the third conductive portion define a first electrode;

selectively removing the dielectric material between the first conductive portion and the second conductive portion to form an opening defined by the first conductive portion and the second conductive portion;

forming an insulting layer within with opening to define a capacitor dielectric layer therefrom;

forming a copper layer overlying the insulating layer to a height above the substantially planar surface to form a second electrode; and

planarizing the copper layer to define the second electrode.

2. The method of claim 1 wherein the planarizing is a chemical mechanical polishing process.

3. The method of claim 1 wherein the first electrode and the second electrode comprise substantially copper material.

4. The method of claim 1 wherein the opening defined by the first portion, the second portion, and the third portion comprises a barrier material defined thereon.

5. The method of claim 1 wherein the first portion and the second portion include a height of about 1 micron and greater.

6. The method of claim 1 wherein the first portion and the second portion along the opening include a spacing of about 100 microns and greater.

7. The method of claim 1 wherein the substantially planar surface is defined by a chemical mechanical polishing process.

8. The method of claim 1 wherein the selecting etching is provided by a plasma etching process comprising a fluorine bearing species followed by a wet etching process using a HF bearing species.

9. The method of claim 1 wherein the HF bearing species has a concentration of about 5% HF or less.

10. The method of claim 8 wherein the plasma etching process has an end point upon exposing a portion of a barrier material defined on the third portion of the conductive material.

11. An integrated circuit device including capacitor structures comprising:

a semiconductor substrate;

a dual damascene structure formed overlying the semiconductor substrate, the dual damascene structure comprising:

a first conductive portion comprising copper material;

a second conductive portion comprising a copper material coupled to the first conductive portion;

a region defined between the first conductive portion and the second conductive portion;

a third conductive portion connecting the second conductive portion and the first portion, the third conductive portion being provided underlying the region;

a substantially planar surface region formed opposing the third conductive portion, the substantially planar surface region comprising a portion of the first conductive portion and a portion of the second conductive portion;

a first capacitor electrode formed from at least the first conductive portion, the second conductive portion, and the third conductive portion;

an opening formed in a portion of the region between the first conductive portion and the second conductive portion;

a capacitor insulting layer formed within the opening in the region;

a planarized copper layer overlying the insulating layer, the planarized copper layer including a surface region at a height at about the substantially planar surface region; and

a second electrode formed from a portion of the planarized copper layer.

12. The method of claim 11 wherein the planarized copper layer is provided by chemical mechanical polishing.

13. The method of claim 11 wherein the first electrode and the second electrode comprise substantially copper material.

14. The method of claim 11 wherein the opening formed by the first portion, the second portion, and the third portion comprises a barrier material defined thereon.

15. The method of claim 11 wherein the first portion and the second portion include a height of about 1 micron and greater.

16. The method of claim 11 wherein the opening within the region has a spacing of about 100 microns and greater.

17. The method of claim 11 wherein the first conductive portion comprises a first plug region and an overlying first layer region and the second conductive portion comprises a first plug region and an overlying first layer region.